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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,846	01/15/2004	John E. Barth JR.	FIS920030409US1	5081
7590	02/03/2005		EXAMINER	
H. Daniel Schnurmann Intellectual Property Law IBM Corporation, Dept. 18G Building 300-482, 2070 Route 52 Hopewell Junction, NY 12533			MAI, SON LUU	
			ART UNIT	PAPER NUMBER
			2827	
			DATE MAILED: 02/03/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/757,846	BARTH ET AL.
	Examiner	Art Unit
	Son L. Mai	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 15 January 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4, 6-12 and 14-18 is/are rejected.
- 7) Claim(s) 5 and 13 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 15 January 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date: _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 4, line 1, "SARM" should be --SRAM--. And in line 5, "TADD" should be --TBADD--.

On page 5, line 17, "SARM » should be --SRAM--.

On page 7, line 5, the article "a" before "applying" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 6-12, 14-16 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 4, the recitation "said first address" in line 1, lacks antecedent basis in the claim. It appears that Applicants refer to the first word address in claim 1.

As for claim 6, "said first memory array" in line 2 and "said second memory array" in line 3, lack antecedent bases in the claim.

As for claim 9, "said third memory array" in line 3, lacks antecedent basis in the claim.

As for claim 14, "said refresh bank", "said memory access bank", and "said at least one more refresh bank [backs]" lack antecedent bases.

As for claim 15, "the random access cycle time" in line 3, lacks antecedent basis in the claim.

Claims 7-12 and 14-16 are rejected because in their dependency they include the limitations of claim 6.

As for claim 18, the recitation "said first address" in line 1, lacks antecedent basis in the claim. It appears that Applicants refer to the first word address in claim 17.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4 and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Agata (U.S. Patent 6,563,757).

Regarding claim 1, Agata discloses a semiconductor memory (figure 3) comprising: a plurality of memory arrays (11), each of which comprises a plurality of memory cells arranged in a matrix and controlled by a row address counter (41) uniquely assigned to each of said memory arrays, said row address counter generating a first word address (refresh address; column 6, lines 1-2); and means (13) for enabling a refresh operation in said memory cells, said memory cells being identified by said first word address when a refresh command is issued to a corresponding memory array.

Regarding claim 2, Agata further teaches each of said memory arrays further comprises a second word address (row address from ROW PREDECODER 16) common to at least two of said memory arrays, and wherein an enabling means (13) enables a memory access operation (read or write) in said memory cells, said memory cells being identified by said second word address when a memory access command is issued to a corresponding memory array (column 4, lines 51-67).

Regarding claim 3, Agata teaches the refresh command is provided by a refresh bank select signal (signal from CONTROL CIRCUIT 13 to SELECTOR 31) to a corresponding memory array.

Regarding claim 4, Agata teaches the first [word] address is updated when said refresh operation has been completed, by incrementing said row address counter (column 6, lines 58-62).

Regarding claim 17, Agata teaches a semiconductor memory device (figure 3) comprising: a plurality of memory arrays (11), each of said memory arrays comprising a plurality of memory cells arranged in a matrix and controlled by a row address counter (41) uniquely assigned to each of said each memory arrays; said row address counter generating a first word address (refresh address; column 6, lines 1-2); means (13) enabling a refresh operation in said memory cells, wherein said memory cells are identified by the first word address when a refresh command is provided to a corresponding memory array; a common second address (row address from row predecoder 16) coupling at least two memory arrays; means (31) for selectively coupling said first and said second word addresses to row decoders within each of said

memory arrays, wherein a refresh operation is enabled by said first word address in a first memory array while enabling a memory access operation by said second word address in a second memory array (column 5, lines 18-59).

Regarding claim 18, Agata teaches the first [word] address is updated when said refresh operation has been completed, by incrementing said row address counter (column 6, lines 58-62).

Allowable Subject Matter

6. Claims 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 6-12 and 14-16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the limitations of claim 5 which calls for a memory access command is provided by a bank select signal to a corresponding memory array.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kotani (U.S. Patent US 5555527 A) and Hwang (U.S. Patent US 6819617 B2) teach memory devices having row address decoders assigned for memory arrays.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01-27-05


Son L. Mai
Primary Examiner
Art Unit 2818